

## $\mu$ A78xx Fixed Positive Voltage Regulators

### 1 Features

- 3-Terminal Regulators
- Available in fixed 5-V/8-V/10-V/12-V/15-V/24-V options
- Output Current up to 1.5 A
- Internal Thermal-Overload Protection
- High Power-Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Capacitor Not Needed for Stability

### 2 Applications

- On-card Regulation
- Portable Devices
- Computing & Servers
- Telecommunications

### 3 Description

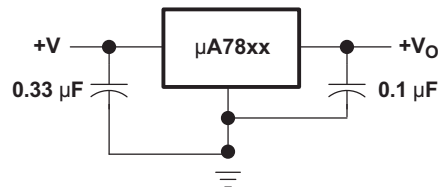
This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current-limiting and thermal-shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents, and also can be used as the power-pass element in precision regulators.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
$\mu$ A78xx	TO-220 (3)	10.16 mm x 8.82 mm
	TO-220 (3)	10.16 mm x 8.82 mm
	TO-263 (3)	10.06 mm x 9.02 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Detailed Description</b> .....	<b>11</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Overview .....	11
<b>3 Description</b> .....	<b>1</b>	8.2 Functional Schematic.....	11
<b>4 Simplified Schematic</b> .....	<b>1</b>	8.3 Feature Description.....	11
<b>5 Revision History</b> .....	<b>2</b>	8.4 Device Functional Modes.....	11
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>9 Application and Implementation</b> .....	<b>12</b>
<b>7 Specifications</b> .....	<b>4</b>	9.1 Application Information.....	12
7.1 Absolute Maximum Ratings .....	4	9.2 Typical Application .....	12
7.2 ESD Ratings .....	4	<b>10 Power Supply Recommendations</b> .....	<b>14</b>
7.3 Recommended Operating Conditions.....	4	<b>11 Layout</b> .....	<b>15</b>
7.4 Thermal Information .....	4	11.1 Layout Guidelines .....	15
7.5 Electrical Characteristics — uA7805.....	5	11.2 Layout Example .....	15
7.6 Electrical Characteristics — uA7808.....	6	<b>12 Device and Documentation Support</b> .....	<b>15</b>
7.7 Electrical Characteristics — uA7810.....	7	12.1 Related Links .....	15
7.8 Electrical Characteristics — uA7812 .....	8	12.2 Trademarks .....	15
7.9 Electrical Characteristics — uA7815.....	9	12.3 Electrostatic Discharge Caution.....	15
7.10 Electrical Characteristics — uA7824.....	10	12.4 Glossary .....	15
7.11 Typical Characteristics .....	10	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>15</b>

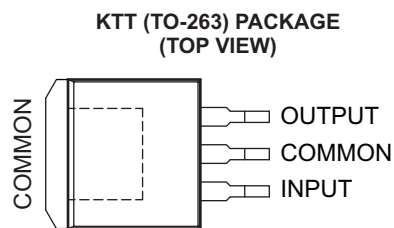
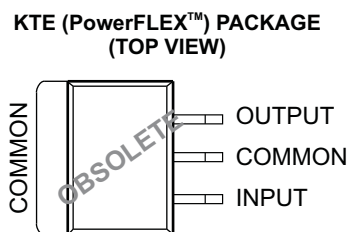
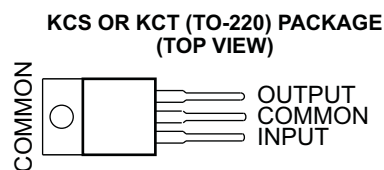
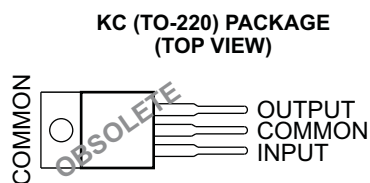
## 5 Revision History

### Changes from Revision O (August 2012) to Revision P

Page

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... 1
- Deleted *Ordering Information* table. .... 1

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
COMMON	2	—	Ground
INPUT	1	I	Supply Input
OUTPUT	3	O	Voltage Output

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>I</sub>	Input voltage	μA7824C	40	V	
		All others	35		
T <sub>J</sub>	Operating virtual junction temperature		150	°C	
	Lead temperature	1,6 mm (1/16 in) from case for 10 s	260	°C	
T <sub>stg</sub>	Storage temperature range		–65	150	°C

### 7.2 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>I</sub>	Input voltage	μA7805	7	25	V
		μA7808	10.5	25	
		μA7810	12.5	28	
		μA7812	14.5	30	
		μA7815	17.5	30	
		μA7824	27	38	
I <sub>O</sub>	Output current		1.5	A	
T <sub>J</sub>	Operating virtual junction temperature	0	125	°C	

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	μA78XX			UNIT	
	KTE	KCS, KCT, KC	KTT		
	3 PINS	3 PINS	3 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	23	19	25.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	3	17	18	
R <sub>θJP(top)</sub>	Junction-to-exposed-pad thermal resistance	2.7	3	1.94	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 7.5 Electrical Characteristics — uA7805

 at specified virtual junction temperature,  $V_I = 10\text{ V}$ ,  $I_O = 500\text{ mA}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$ <sup>(1)</sup>	uA7805C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$ , $V_I = 7\text{ V to }20\text{ V}$ , $P_D \leq 15\text{ W}$	25°C	4.8	5	5.2	V
		0°C to 125°C	4.75		5.25	
Input voltage regulation	$V_I = 7\text{ V to }25\text{ V}$	25°C		3	100	mV
	$V_I = 8\text{ V to }12\text{ V}$			1	50	
Ripple rejection <sup>(2)</sup>	$V_I = 8\text{ V to }12\text{ V}$ , $f = 120\text{ Hz}$	0°C to 125°C	62	78		dB
	$V_I = 8\text{ V to }12\text{ V}$ , $f = 120\text{ Hz (KCT)}$			68		
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C		15	100	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			5	50	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C		0.017		$\Omega$
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-1.1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		40		$\mu\text{V}$
Dropout voltage	$I_O = 1\text{ A}$	25°C		2		V
Bias current		25°C		4.2	8	mA
Bias current change	$V_I = 7\text{ V to }25\text{ V}$	0°C to 125°C			1.3	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- $\mu\text{F}$  capacitor across the input and a 0.1- $\mu\text{F}$  capacitor across the output.
- (2) This parameter is validated by design and verified during product characterization. It is not tested in production.

## 7.6 Electrical Characteristics — uA7808

at specified virtual junction temperature,  $V_I = 14\text{ V}$ ,  $I_O = 500\text{ mA}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$ <sup>(1)</sup>	$\mu\text{A7808C}$			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$ , $V_I = 10.5\text{ V to }23\text{ V}$ , $P_D \leq 15\text{ W}$	25°C	7.7	8	8.3	V
		0°C to 125°C	7.6		8.4	
Input voltage regulation	$V_I = 10.5\text{ V to }25\text{ V}$	25°C		6	160	mV
	$V_I = 11\text{ V to }17\text{ V}$			2	80	
Ripple rejection <sup>(2)</sup>	$V_I = 11.5\text{ V to }21.5\text{ V}$ , $f = 120\text{ Hz}$	0°C to 125°C	55	72		dB
	$V_I = 11.5\text{ V to }21.5\text{ V}$ , $f = 120\text{ Hz}$ (KCT)			62		
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C		12	160	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			4	80	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C		0.016		$\Omega$
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-0.8		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		52		$\mu\text{V}$
Dropout voltage	$I_O = 1\text{ A}$	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	$V_I = 10.5\text{ V to }25\text{ V}$	0°C to 125°C			1	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- $\mu\text{F}$  capacitor across the input and a 0.1- $\mu\text{F}$  capacitor across the output.
- (2) This parameter is validated by design and verified during product characterization. It is not tested in production.

## 7.7 Electrical Characteristics — uA7810

at specified virtual junction temperature,  $V_I = 17\text{ V}$ ,  $I_O = 500\text{ mA}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$ <sup>(1)</sup>	uA7810C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$ , $V_I = 12.5\text{ V to }25\text{ V}$ , $P_D \leq 15\text{ W}$	25°C	9.6	10	10.4	V
		0°C to 125°C	9.5		10.5	
Input voltage regulation	$V_I = 12.5\text{ V to }28\text{ V}$	25°C		7	200	mV
	$V_I = 14\text{ V to }20\text{ V}$			2	100	
Ripple rejection <sup>(2)</sup>	$V_I = 13\text{ V to }23\text{ V}$ , $f = 120\text{ Hz}$	0°C to 125°C	55	71		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C		12	200	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			4	100	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C		0.018		$\Omega$
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		70		$\mu\text{V}$
Dropout voltage	$I_O = 1\text{ A}$	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	$V_I = 12.5\text{ V to }28\text{ V}$	0°C to 125°C			1	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C		400		mA
Peak output current		25°C		2.2		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- $\mu\text{F}$  capacitor across the input and a 0.1- $\mu\text{F}$  capacitor across the output.
- (2) This parameter is validated by design and verified during product characterization. It is not tested in production.

## 7.8 Electrical Characteristics — uA7812

at specified virtual junction temperature,  $V_I = 19\text{ V}$ ,  $I_O = 500\text{ mA}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$ <sup>(1)</sup>	uA7812C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$ , $V_I = 14.5\text{ V to }27\text{ V}$ , $P_D \leq 15\text{ W}$	25°C	11.5	12	12.5	V
		0°C to 125°C	11.4		12.6	
Input voltage regulation	$V_I = 14.5\text{ V to }30\text{ V}$	25°C		10	240	mV
	$V_I = 16\text{ V to }22\text{ V}$			3	120	
Ripple rejection <sup>(2)</sup>	$V_I = 15\text{ V to }25\text{ V}$ , $f = 120\text{ Hz}$	0°C to 125°C	55	71		dB
	$V_I = 15\text{ V to }25\text{ V}$ , $f = 120\text{ Hz (KCT)}$			61		
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C		12	240	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			4	120	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C		0.018		$\Omega$
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		75		$\mu\text{V}$
Dropout voltage	$I_O = 1\text{ A}$	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	$V_I = 14.5\text{ V to }30\text{ V}$	0°C to 125°C			1	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C		350		mA
Peak output current		25°C		2.2		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33- $\mu\text{F}$  capacitor across the input and a 0.1- $\mu\text{F}$  capacitor across the output.
- (2) This parameter is validated by design and verified during product characterization. It is not tested in production.



## 7.9 Electrical Characteristics — uA7815

at specified virtual junction temperature,  $V_I = 23\text{ V}$ ,  $I_O = 500\text{ mA}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$ <sup>(1)</sup>	μA7815C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$ , $V_I = 17.5\text{ V to }30\text{ V}$ , $P_D \leq 15\text{ W}$	25°C	14.4	15	15.6	V
		0°C to 125°C	14.25		15.75	
Input voltage regulation	$V_I = 17.5\text{ V to }30\text{ V}$	25°C		11	300	mV
	$V_I = 20\text{ V to }26\text{ V}$			3	150	
Ripple rejection <sup>(2)</sup>	$V_I = 18.5\text{ V to }28.5\text{ V}$ , $f = 120\text{ Hz}$	0°C to 125°C	54	70		dB
	$V_I = 18.5\text{ V to }28.5\text{ V}$ , $f = 120\text{ Hz}$ (KCT)			60		
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C		12	300	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			4	150	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-1		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		90		μV
Dropout voltage	$I_O = 1\text{ A}$	25°C		2		V
Bias current		25°C		4.4	8	mA
Bias current change	$V_I = 17.5\text{ V to }30\text{ V}$	0°C to 125°C			1	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C		230		mA
Peak output current		25°C		2.1		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.
- (2) This parameter is validated by design and verified during product characterization. It is not tested in production.

## 7.10 Electrical Characteristics — uA7824

at specified virtual junction temperature,  $V_I = 33\text{ V}$ ,  $I_O = 500\text{ mA}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_J$ <sup>(1)</sup>	μA7824C			UNIT
			MIN	TYP	MAX	
Output voltage	$I_O = 5\text{ mA to }1\text{ A}$ , $V_I = 27\text{ V to }38\text{ V}$ , $P_D \leq 15\text{ W}$	25°C	23	24	25	V
		0°C to 125°C	22.8		25.2	
Input voltage regulation	$V_I = 27\text{ V to }38\text{ V}$	25°C		18	480	mV
	$V_I = 30\text{ V to }36\text{ V}$			6	240	
Ripple rejection <sup>(2)</sup>	$V_I = 28\text{ V to }38\text{ V}$ , $f = 120\text{ Hz}$	0°C to 125°C	50	66		dB
Output voltage regulation	$I_O = 5\text{ mA to }1.5\text{ A}$	25°C		12	480	mV
	$I_O = 250\text{ mA to }750\text{ mA}$			4	240	
Output resistance	$f = 1\text{ kHz}$	0°C to 125°C		0.028		Ω
Temperature coefficient of output voltage	$I_O = 5\text{ mA}$	0°C to 125°C		-1.5		mV/°C
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$	25°C		170		μV
Dropout voltage	$I_O = 1\text{ A}$	25°C		2		V
Bias current		25°C		4.6	8	mA
Bias current change	$V_I = 27\text{ V to }38\text{ V}$	0°C to 125°C			1	mA
	$I_O = 5\text{ mA to }1\text{ A}$				0.5	
Short-circuit output current		25°C		150		mA
Peak output current		25°C		2.1		A

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.
- (2) This parameter is validated by design and verified during product characterization. It is not tested in production.

## 7.11 Typical Characteristics

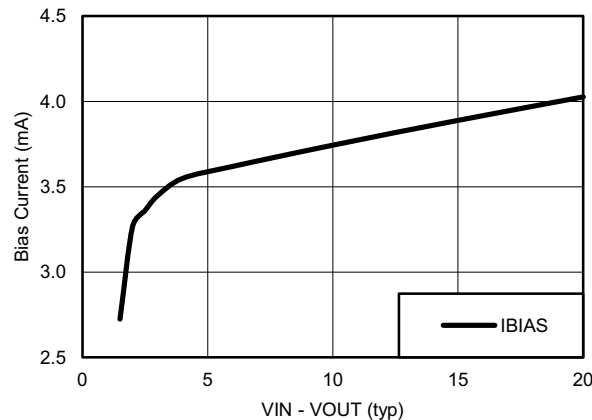


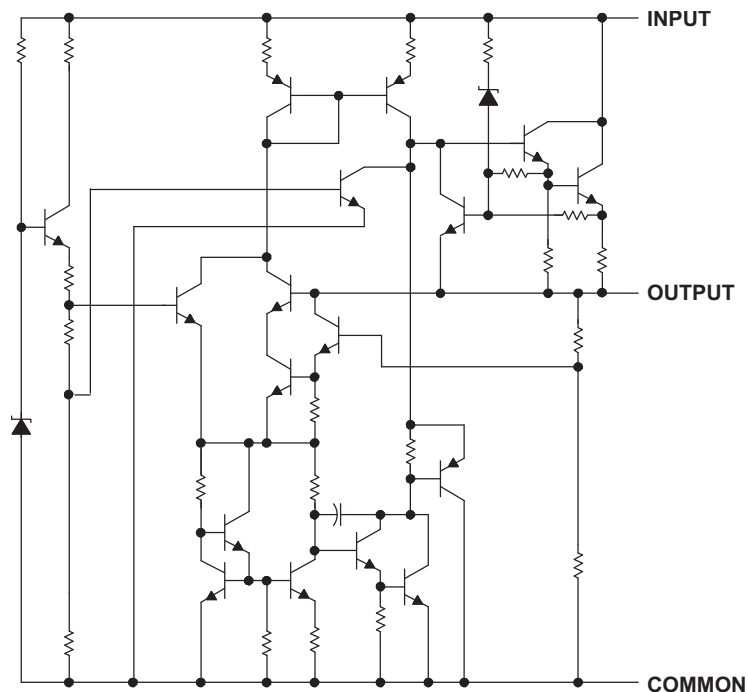
Figure 1. μA7805 Bias Current vs Voltage Differential at 25°C

## 8 Detailed Description

### 8.1 Overview

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current-limiting and thermal-shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents, and also can be used as the power-pass element in precision regulators.

### 8.2 Functional Schematic



### 8.3 Feature Description

#### 8.3.1 Thermal Overload

When the die temperature increases to unwanted levels, the device will reduce the output current to lower its temperature. Under heavy loads, the device may alternate between on and off output states to regulate temperature.

#### 8.3.2 Short-Circuit Current Limiting

In the event of a short circuit, the device will limit its own current to safe levels by lowering the bias voltage of internal pass transistors. If the device becomes overheated, the thermal overload protection will take over.

### 8.4 Device Functional Modes

#### 8.4.1 Fixed-Output Mode

These devices are available in fixed-output voltages. See the orderable part list for the desired output.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The following section shows application details of the  $\mu$ A78xx as a linear regulator.

### 9.2 Typical Application

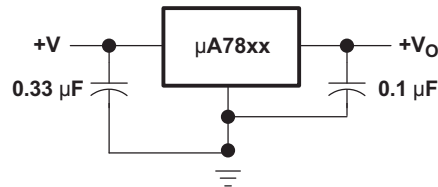


Figure 2. Fixed-Output Regulator

#### 9.2.1 Design Requirements

- Input supply capacitor recommended for filtering noise on the input
- Output supply decoupling capacitor for stabilizing the output

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Operation With a Load Common to a Voltage of Opposite Polarity

In many cases, a regulator powers a load that is not connected to ground but, instead, is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 3. This protects the regulator from output polarity reversals during startup and short-circuit operation.

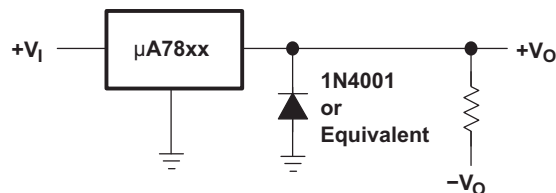


Figure 3. Output Polarity-Reversal-Protection Circuit

##### 9.2.2.2 Reverse-Bias Protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This can occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series-pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be used as shown in Figure 4.

### Typical Application (continued)

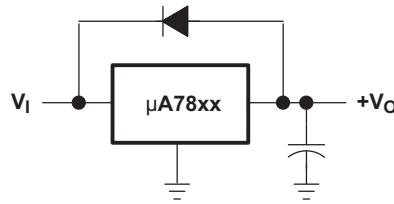


Figure 4. Reverse-Bias-Protection Circuit

### 9.2.3 Application Curves

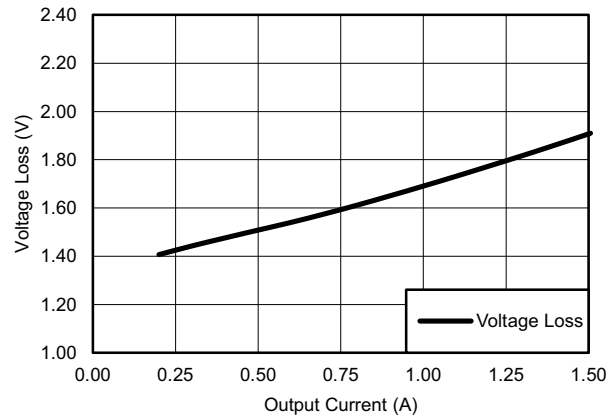


Figure 5. μA7805 Voltage Loss vs Output Current at 25°C

### 9.2.4 General Configurations

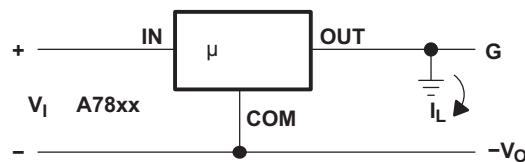
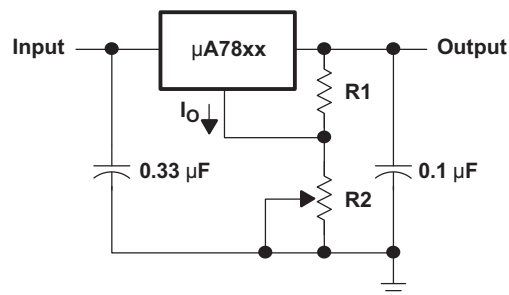


Figure 6. Positive Regulator in Negative Configuration ( $V_I$  Must Float)



A: The following formula is used when  $V_{xx}$  is the nominal output voltage (output to common) of the fixed regulators

$$V_o = V_{xx} + \left( \frac{V_{xx}}{R1} + I_o \right) R2$$

Figure 7. Adjustable-Output Regulator

## Typical Application (continued)

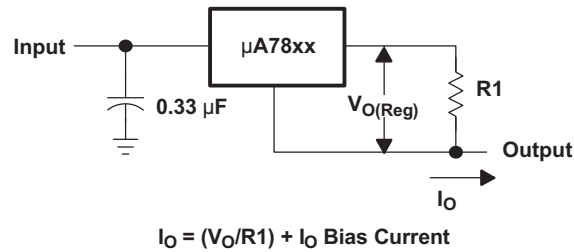


Figure 8. Current Regulator



Figure 9. Regulated Dual Supply

## 10 Power Supply Recommendations

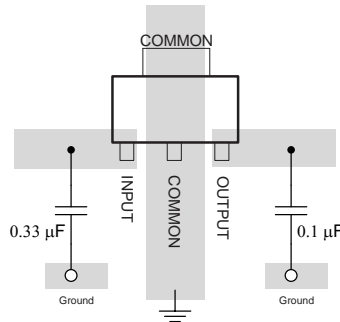
See [Recommended Operating Conditions](#) for the recommended power supply voltages for each variation of the  $\mu A78xx$  device. Different orderable part numbers will be able to tolerate different levels of voltage. It is also recommended to have a decoupling capacitor on the output of the  $\mu A78xx$  device's power supply to limit noise on the device input.

## 11 Layout

### 11.1 Layout Guidelines

Keep trace widths large enough to eliminate problematic I×R voltage drops at the input and output terminals. Input decoupling capacitors should be placed as close to the μA78XX as possible.

### 11.2 Layout Example



**Figure 10. Layout Diagram**

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
μA7805	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
uA7808	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
uA7810	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
uA7812	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
uA7815	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
uA7924	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Trademarks

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA7805CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7805C	<a href="#">Samples</a>
UA7805CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7805C	<a href="#">Samples</a>
UA7805CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7805C	<a href="#">Samples</a>
UA7805CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7805C	<a href="#">Samples</a>
UA7805CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7805C	<a href="#">Samples</a>
UA7808CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7808C	<a href="#">Samples</a>
UA7808CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7808C	<a href="#">Samples</a>
UA7808CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7808C	<a href="#">Samples</a>
UA7808CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7808C	<a href="#">Samples</a>
UA7808CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7808C	<a href="#">Samples</a>
UA7810-W	ACTIVE	WAFERSALE	YS	0	3952	TBD	Call TI	Call TI			<a href="#">Samples</a>
UA7810CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7810C	<a href="#">Samples</a>
UA7810CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7810C	<a href="#">Samples</a>
UA7810CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7810C	<a href="#">Samples</a>
UA7810CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7810C	<a href="#">Samples</a>
UA7812CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7812C	<a href="#">Samples</a>
UA7812CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7812C	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA7812CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7812C	<a href="#">Samples</a>
UA7812CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7812C	<a href="#">Samples</a>
UA7812CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7812C	<a href="#">Samples</a>
UA7815CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7815C	<a href="#">Samples</a>
UA7815CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7815C	<a href="#">Samples</a>
UA7815CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7815C	<a href="#">Samples</a>
UA7815CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7815C	<a href="#">Samples</a>
UA7824CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7824C	<a href="#">Samples</a>
UA7824CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7824C	<a href="#">Samples</a>
UA7824CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7824C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA7805CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7805CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.1	4.9	16.0	24.0	Q2
UA7808CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7810CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7812CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7812CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.1	4.9	16.0	24.0	Q2
UA7815CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7824CKTTR	DDPAK/TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

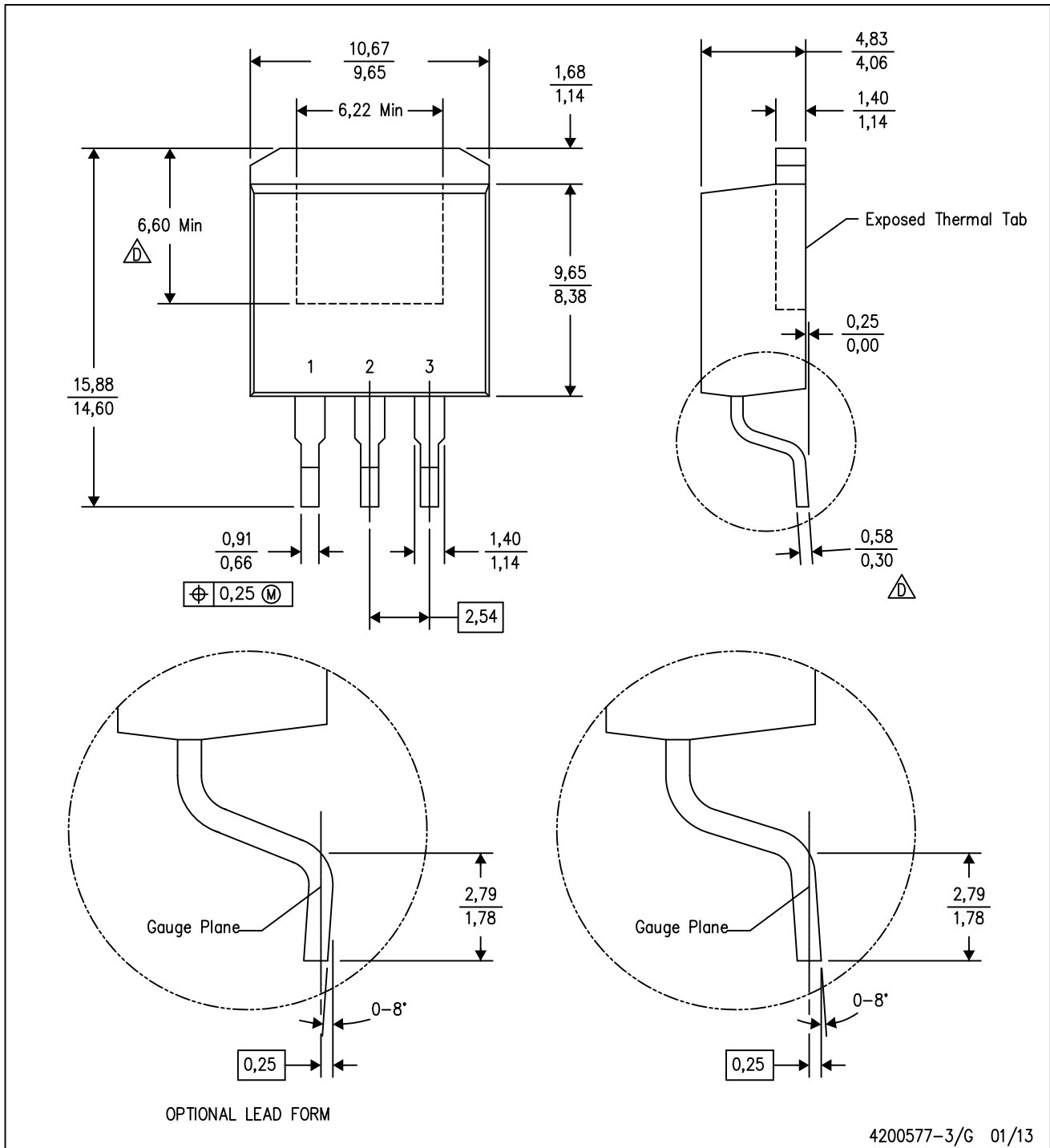
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA7805CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7805CKTTR	DDPAK/TO-263	KTT	3	500	350.0	334.0	47.0
UA7808CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7810CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7812CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7812CKTTR	DDPAK/TO-263	KTT	3	500	350.0	334.0	47.0
UA7815CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7824CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



4200577-3/G 01/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- $\triangle$  Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

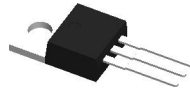
KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-SM-782 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
  - This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

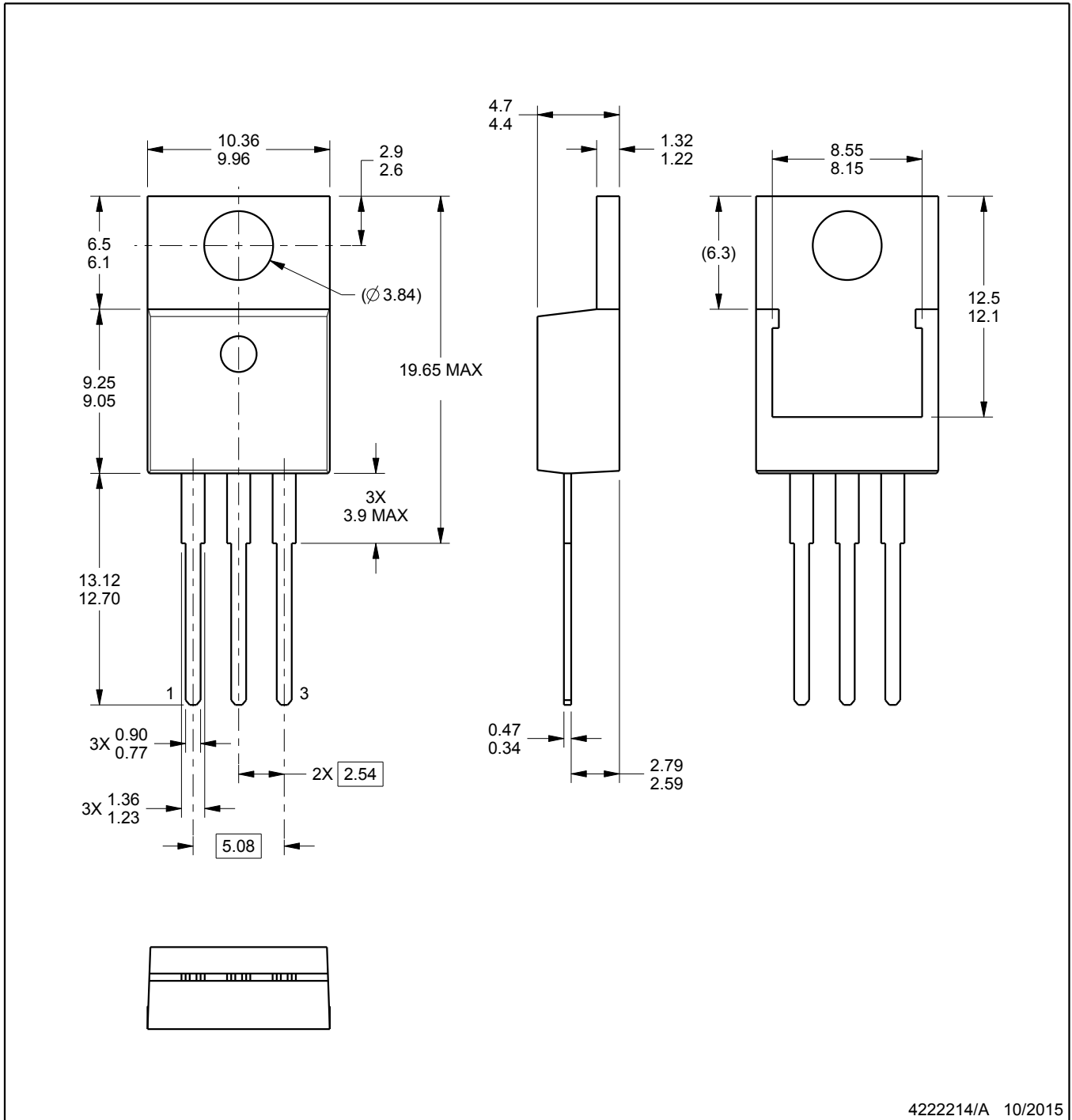
# KCS0003B



# PACKAGE OUTLINE

TO-220 - 19.65 mm max height

TO-220



4222214/A 10/2015

### NOTES:

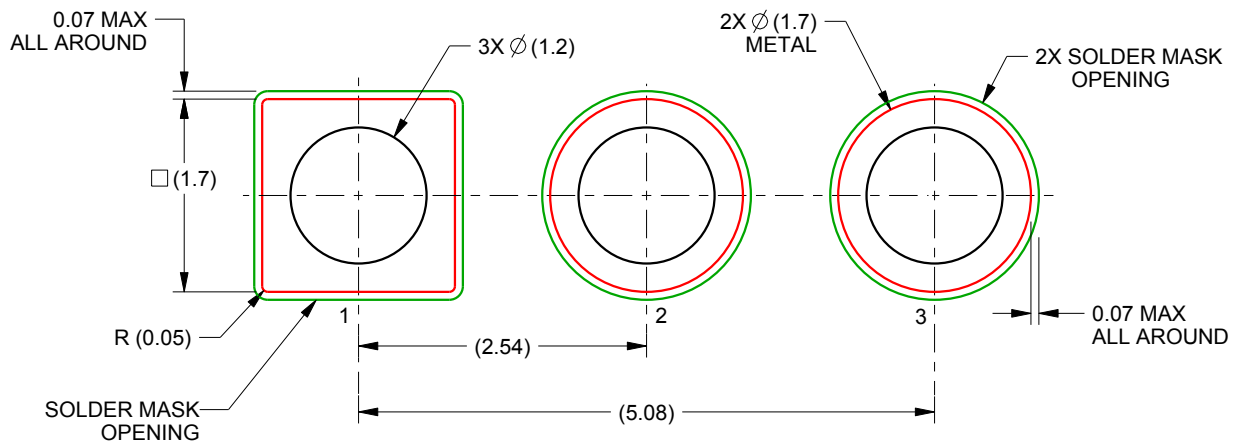
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

# EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220



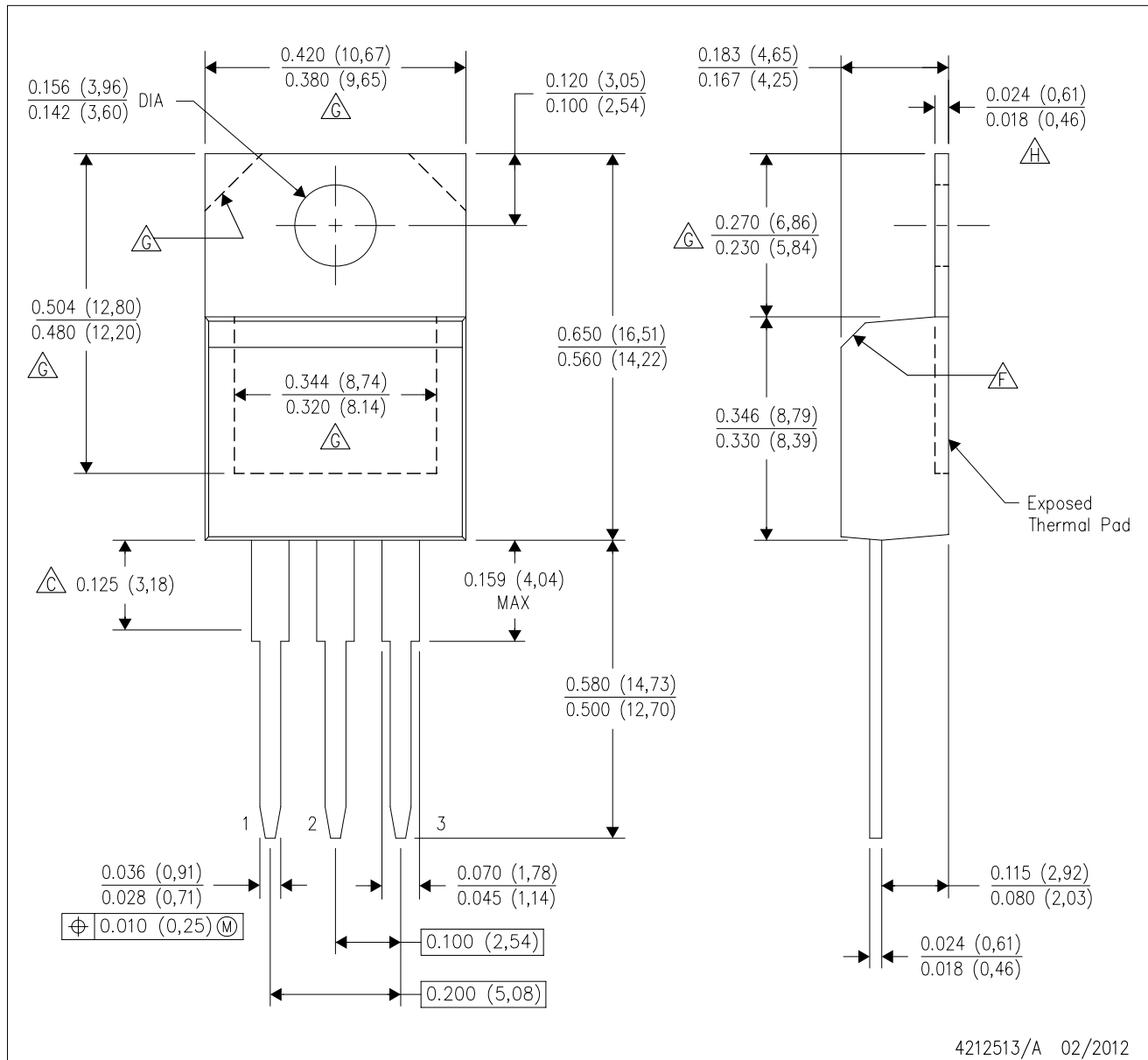
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 15X

4222214/A 10/2015



KCT (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



4212513/A 02/2012

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Lead dimensions are not controlled within this area.
  - D. All lead dimensions apply before solder dip.
  - E. The center lead is in electrical contact with the mounting tab.
  - F. The chamfer is optional.
  - G. Thermal pad contour optional within these dimensions.
  - H. Falls within JEDEC TO-220 variation AB, except minimum tab thickness.

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