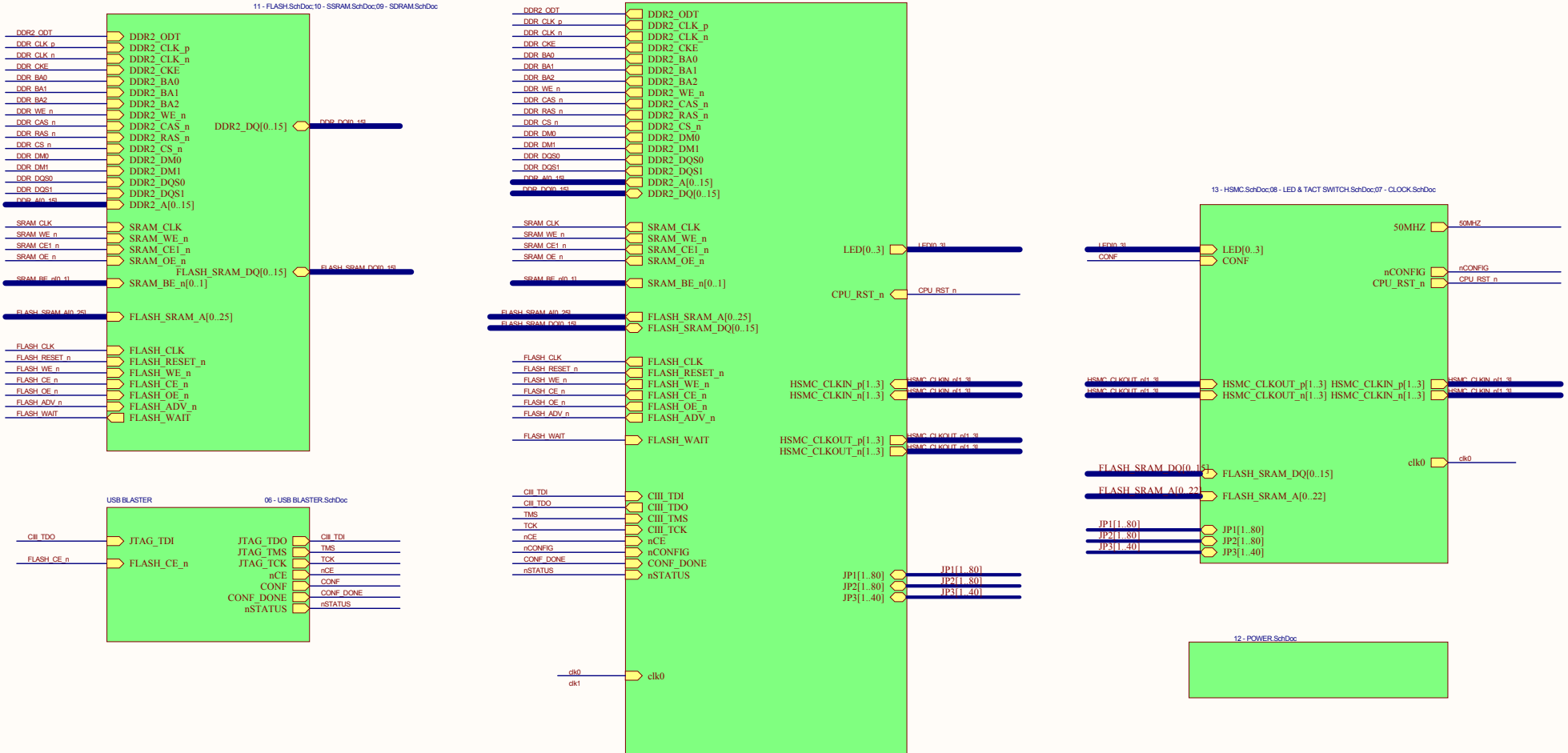


05 - POWER & CONFIG.SchDoc:04 - BANK7 & BANK8.SchDoc:03 - BANK5 & BANK6.SchDoc:02 - BANK3 & BANK4.SchDoc:01 - BANK1 & BANK2.SchDoc



Title		
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A	TOP LEVEL	1/2
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U1A

BANK 1

IO, DIFFIO_L1p	G4	G4	JP2_74
IO, DIFFIO_L1n	G3	G3	JP2_75
IO, DIFFIO_L2p, (DQ2L)/(DQ1L)/(DQ1L)	B2	B2	JP2_66
IO, DIFFIO_L2n, (DQ2L)/(DQ1L)/(DQ1L)	B1	B1	JP2_65
IO, VREFB1N0	G5	G5	JP2_72
IO, DIFFIO_L4p, (nRESET), (DQ2L)/(DQ1L)/(DQ1L)	F4		FLASH_RESET_n
IO, DIFFIO_L4n, (DQ2L)/(DQ1L)/(DQ1L)	E3	E3	JP2_73
IO, DIFFIO_L7p, (DQS2L/CQ3L,CDPCLK0)/(DQS2L/CQ3L,CDPCLK0)	C2	C2	JP2_64
IO, DIFFIO_L7n, (DQ2L)/(DQ1L)/(DQ1L)	C1	C1	JP2_63
IO, DIFFIO_L8p, (DQ2L)/(DQ1L)/(DQ1L)	D2	D2	JP2_62
IO, DIFFIO_L8n, (DATA1, ASDO)	D1		FLASH_SRAM_DQ[
IO, VREFB1N1	H7	H7	JP2_69
IO, DIFFIO_L9p, (DQ2L)/(DQ1L)/(DQ1L)	H6	H6	JP2_71
IO, DIFFIO_L9n, (DQ2L)/(DQ1L)/(DQ1L)	J6	J6	JP2_68
IO, DIFFIO_L10p, (FLASH_nCE, nCS0)	F2		FLASH_CE_n
IO, DIFFIO_L10n, (DQ1L)/(DQ1L)	E1	E1	JP2_61
IO, DIFFIO_L12p, (DM2L)/(DM1L0/BWS#1L0)/(DM1L0/BWS#1L0)	F2	F2	JP2_60
IO, DIFFIO_L12n, (DQ1L)/(DQ1L)	F1	F1	JP2_59
IO, VREFB1N2	H5	H5	JP2_70
IO, DIFFIO_L20p	J8	J8	JP2_50
IO, DIFFIO_L20n	J8	J8	JP2_52
IO, DIFFIO_L21p	J7	J7	JP2_67
IO, DIFFIO_L21n	J7	J7	JP2_51
IO, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)	J3	J3	JP2_54
IO, DIFFIO_L23p, (DQ0L)/(DQ1L)/(DQ1L)	H2	H2	JP2_58
IO, DIFFIO_L23n, (DQ0L)/(DQ1L)/(DQ1L)	H1	H1	JP2_57
IO, VREFB1N3	J5	J5	JP2_53
IO, DIFFIO_L24p, (DQ0L)/(DQ1L)/(DQ1L)	J2	J2	JP2_56
IO, DIFFIO_L24n, (DQ0L)/(DQ1L)/(DQ1L)	J1	J1	JP2_55

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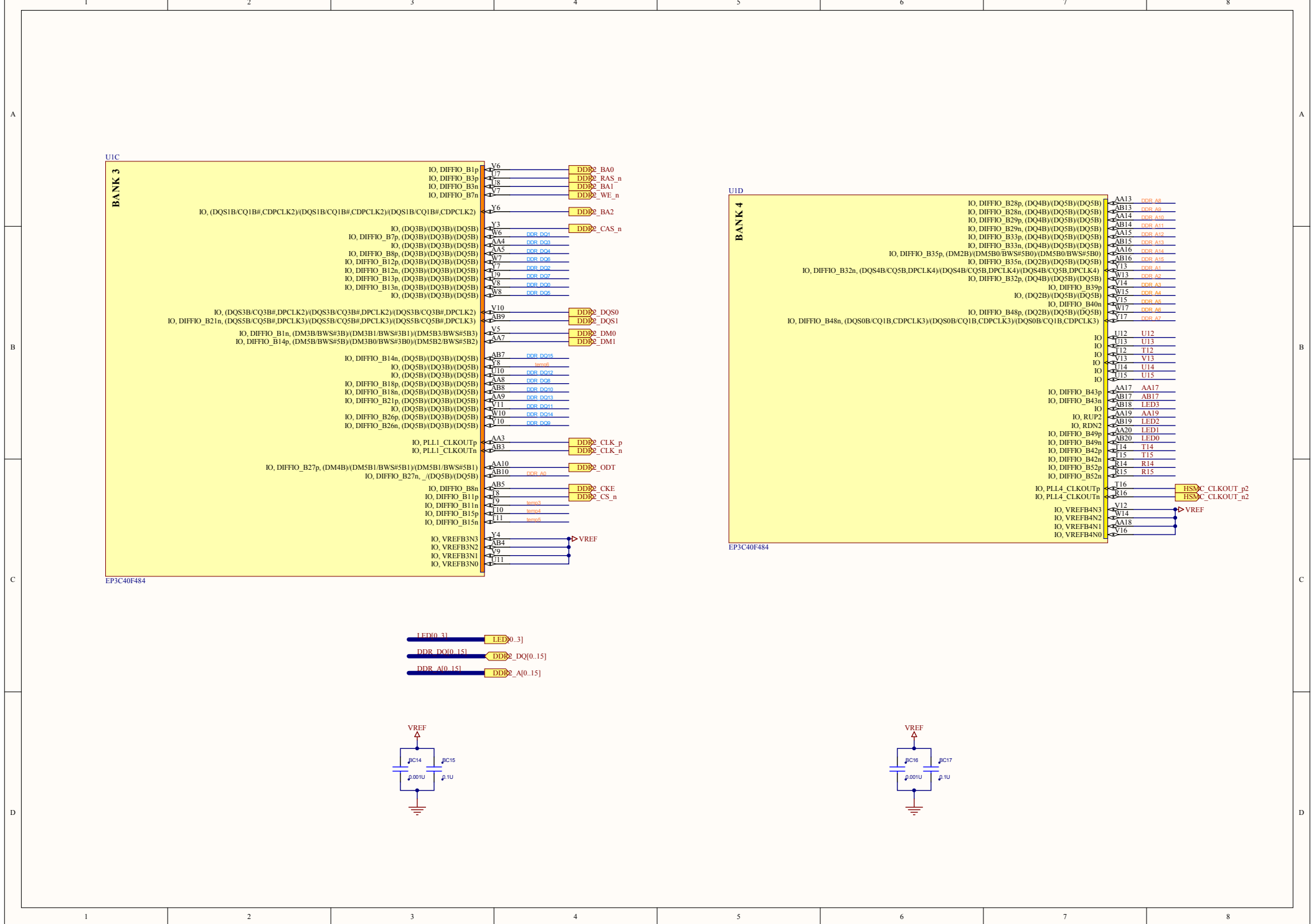


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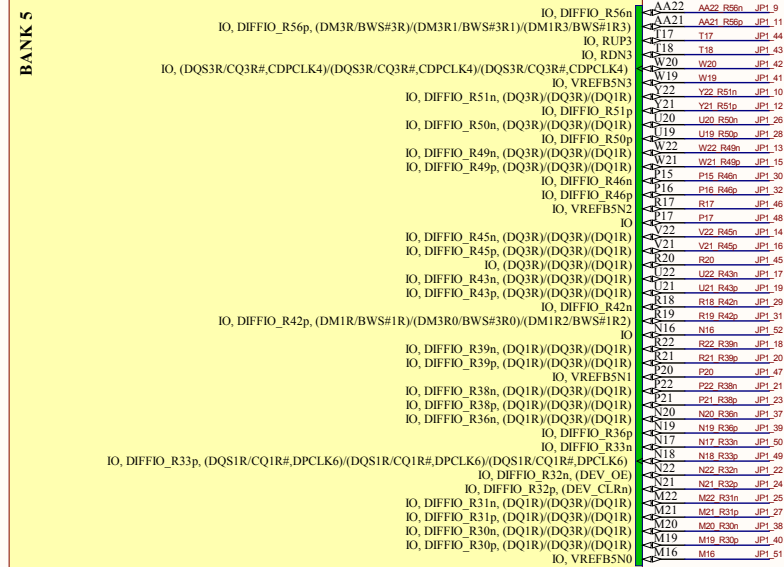
BANK 2

IO, DIFFIO_L26p, (DQ0L)/(DQ1L)/(DQ1L)	L6	L6	JP2_49
IO, DIFFIO_L26n, (DQ0L)/(DQ1L)/(DQ1L)	M6	M6	JP2_45
IO, DIFFIO_L27p, (DQ0L)/(DQ1L)/(DQ1L)	M2	M2	JP2_22
IO, DIFFIO_L27n, (DQ1L)/(DQ1L)	M1	M1	JP2_24
IO, DIFFIO_L28p, (DM0L)/(DM1L1/BWS#1L1)/(DM1L1/BWS#1L1)	M4	M4	JP2_30
IO, DIFFIO_L28n, (DQ1L)/(DQ3L)/(DQ1L)	M3	M3	JP2_32
IO, DIFFIO_L29p, (DQ1L)/(DQ3L)/(DQ1L)	N2	N2	JP2_17
IO, DIFFIO_L29n, (DQ1L)/(DQ3L)/(DQ1L)	N1	N1	JP2_19
IO, VREFB2N0	L7	L7	JP2_46
IO, DIFFIO_L32p, (DQ1L)/(DQ3L)/(DQ1L)	M5	M5	JP2_43
IO, DIFFIO_L32n, (DQ1L)/(DQ3L)/(DQ1L)	P2	P2	JP2_18
IO, DIFFIO_L33p, (DQ1L)/(DQ3L)/(DQ1L)	P1	P1	JP2_20
IO, DIFFIO_L33n, (DQ1L)/(DQ3L)/(DQ1L)	R2	R2	JP2_13
IO, DIFFIO_L33n, (DQ1L)/(DQ3L)/(DQ1L)	R1	R1	JP2_15
IO, (DQ1L)/(DQ3L)/(DQ1L)	N5	N5	JP2_44
IO, DIFFIO_L34p, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)	P4	P4	JP2_27
IO, DIFFIO_L34n, (DQ1L)/(DQ3L)/(DQ1L)	P3	P3	JP2_25
IO, DIFFIO_L35p, (DM1L/BWS#1L1)/(DM3L0/BWS#3L0)/(DM1L2/BWS#1L2)	L1	L1	JP2_16
IO, DIFFIO_L35n, (DQ3L)/(DQ3L)/(DQ1L)	V2	V2	JP2_9
IO, DIFFIO_L38p, (DQ3L)/(DQ3L)/(DQ1L)	V1	V1	JP2_11
IO, DIFFIO_L38n, (DQ3L)/(DQ3L)/(DQ1L)	P5	P5	JP2_41
IO, VREFB2N1	N6	N6	JP2_29
IO, DIFFIO_L41p, (DQ3L)/(DQ3L)/(DQ1L)	M7	M7	JP2_31
IO, DIFFIO_L41n	M8	M8	JP2_34
IO, DIFFIO_L42p	N2	N2	JP2_10
IO, DIFFIO_L42n	V2	V2	JP2_12
IO, DIFFIO_L44p, (DQ3L)/(DQ3L)/(DQ1L)	V1	V1	JP2_5
IO, DIFFIO_L44n, (DQ3L)/(DQ3L)/(DQ1L)	Y2	Y2	JP2_5
IO, DIFFIO_L45p, (DQ3L)/(DQ3L)/(DQ1L)	Y1	Y1	JP2_7
IO, DIFFIO_L45n, (DQ3L)/(DQ3L)/(DQ1L)	T3	T3	JP2_40
IO, VREFB2N2	N7	N7	JP2_26
IO, DIFFIO_L49p	P7	P7	JP2_28
IO, DIFFIO_L49n	A2	A2	JP2_9
IO, DIFFIO_L50p	A1	A1	JP2_8
IO, DIFFIO_L50n, (DQ3L)/(DQ3L)/(DQ1L)	V4	V4	JP2_33
IO, RUP1	V3	V3	JP2_35
IO, RDN1	P6	P6	JP2_42
IO, (DM3L/BWS#3L1)/(DM3L1/BWS#3L1)/(DM1L3/BWS#1L3)	T5	T5	JP2_38
IO, (DQS3L/CQ3L#,CDPCLK1)/(DQS3L/CQ3L#,CDPCLK1)	T4	T4	JP2_37
IO, VREFB2N3	R5	R5	JP2_39
IO, DIFFIO_L53p	R6	R6	JP2_47
IO, DIFFIO_L53n	R7	R7	JP2_21
	T7	T7	JP2_23

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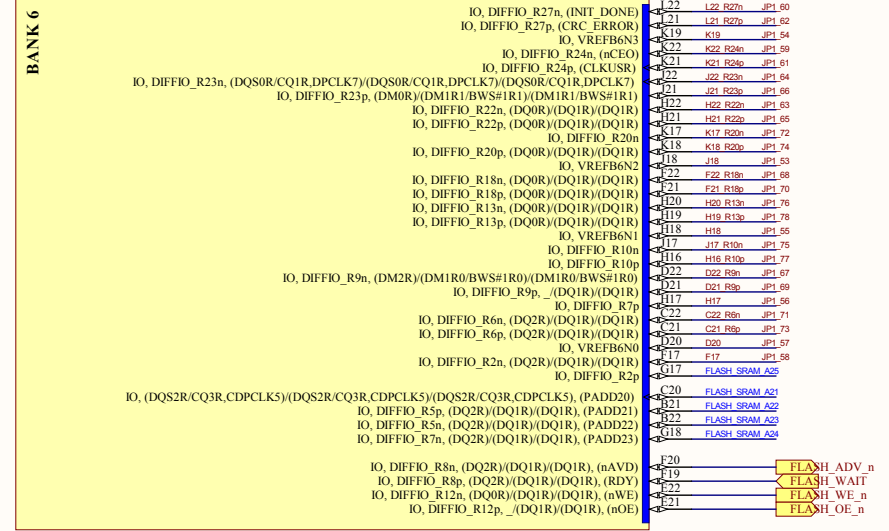


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UIF



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JP1[1..80] JP1\_11..80

JP2[1..80] JP2\_11..80

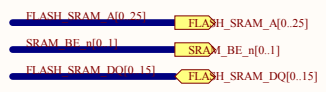
FLASH\_SRAM\_A[0..25] FLASH\_SRAM\_A[0..25]

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BANK 7

IO, DIFFIO\_T45p, (PADD0) B18 FLASH\_SRAM\_A1  
 IO, DIFFIO\_T41n, (DQ2T)(DQ5T)(DQ5T), (PADD1) B17 FLASH\_SRAM\_A2  
 IO, DIFFIO\_T41p, (DQ5T)(DQ5T), (PADD2) B17 FLASH\_SRAM\_A2  
 IO, (DQ4T)(DQ5T)(DQ5T), (PADD3) B17 FLASH\_SRAM\_A2  
 IO, DIFFIO\_T36n, (DQ4T)(DQ5T)(DQ5T), (PADD4) B14 FLASH\_SRAM\_A6  
 IO, DIFFIO\_T36p, (DQ4T)(DQ5T)(DQ5T), (PADD5) A15 FLASH\_SRAM\_A6  
 IO, DIFFIO\_T35n, (PADD6) B15 FLASH\_SRAM\_A7  
 IO, DIFFIO\_T35p, (DQ4T)(DQ5T)(DQ5T), (PADD7) B13 FLASH\_SRAM\_A8  
 IO, DIFFIO\_T35n, (DQ4T)(DQ5T)(DQ5T), (PADD8) B13 FLASH\_SRAM\_A8  
 IO, DIFFIO\_T31n, (DQ4T)(DQ5T)(DQ5T), (PADD9) B14 FLASH\_SRAM\_A10  
 IO, DIFFIO\_T31p, (DQ4T)(DQ5T)(DQ5T), (PADD10) B13 FLASH\_SRAM\_A12  
 IO, DIFFIO\_T29n, (DQ4T)(DQ5T)(DQ5T), (PADD11) B13 FLASH\_SRAM\_A13  
 IO, DIFFIO\_T29p, (DQ4T)(DQ5T)(DQ5T), (PADD12) B11 FLASH\_SRAM\_A14  
 IO, DIFFIO\_T27p, (DM4T)(DM5T1/BWS#5T1)(DM5T1/BWS#5T1), (PADD14) F11 FLASH\_SRAM\_A15  
 IO, DIFFIO\_T40n, (DM2T)(DM5T0/BWS#5T0)(DM5T0/BWS#5T0) B16 SRAM\_CE1\_n  
 IO, DIFFIO\_T40p, (DQ4T)(DQ5T)(DQ5T) F16 SRAM\_WE\_n  
 IO, DIFFIO\_T51p, (DQ2T)(DQ5T)(DQ5T) E16 JP3\_5  
 IO, DIFFIO\_T50n, (DQ2T)(DQ5T)(DQ5T) E15 JP3\_27  
 IO, DIFFIO\_T50p, E15 JP3\_7  
 IO, DIFFIO\_T49n, E14 JP3\_11  
 IO, DIFFIO\_T49n, (DQ80T/CQ1T,CDPCLK6)(DQ80T/CQ1T,CDPCLK6) F15 JP3\_30  
 IO, DIFFIO\_T48n, (DQ80T/CQ1T,CDPCLK6)(DQ80T/CQ1T,CDPCLK6) F14 JP3\_11  
 IO, DIFFIO\_T48p, F15 JP3\_28  
 IO, VREFB7N0, E17 JP3\_3  
 IO, DIFFIO\_T47n, (DQ2T)(DQ5T)(DQ5T) E19 JP3\_6  
 IO, DIFFIO\_T47p, (DQ2T)(DQ5T)(DQ5T) E19 JP3\_4  
 IO, PLL2\_CLKOUTn, A20 HSMC\_CLKOUT\_p1  
 IO, PLL2\_CLKOUTp, A20 HSMC\_CLKOUT\_n1  
 IO, (DQ2T)(DQ5T)(DQ5T) E17 JP3\_8  
 IO, RUP4, B19 JP3\_23  
 IO, RDN4, A19 JP3\_24  
 IO, DIFFIO\_T45n, (DQ2T)(DQ5T)(DQ5T) A18 JP3\_26  
 IO, VREFB7N1, E15 JP3\_10  
 IO, DIFFIO\_T44n, (DQ2T)(DQ5T)(DQ5T) E15 JP3\_12  
 IO, DIFFIO\_T44p, E14 JP3\_14  
 IO, E13 JP3\_13  
 IO, VREFB7N2, E15 JP3\_9  
 IO, VREFB7N3, E13 JP3\_29  
 IO, (DQ5T)(DQ5T) E12 JP3\_32

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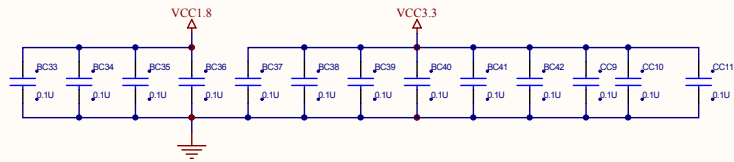
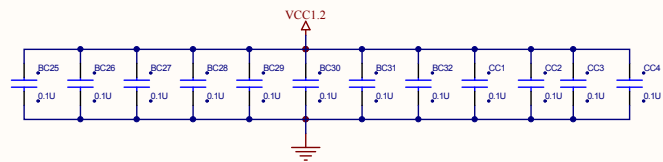
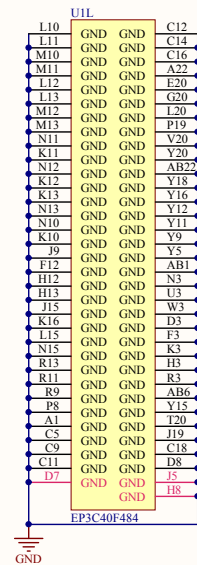
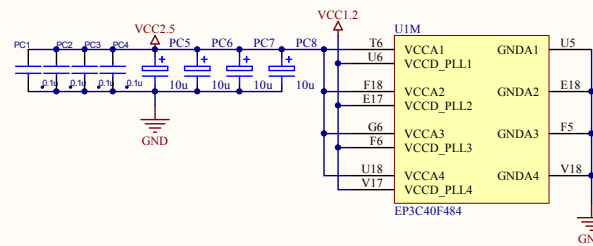
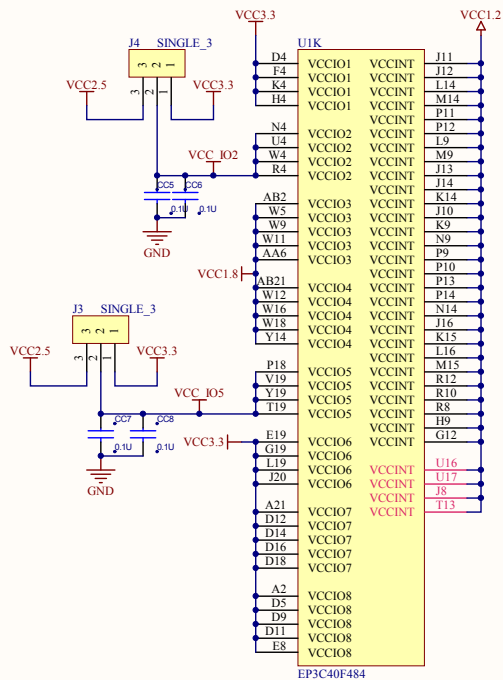
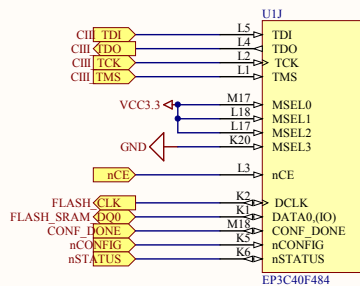


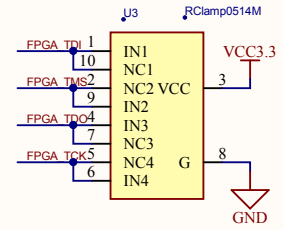
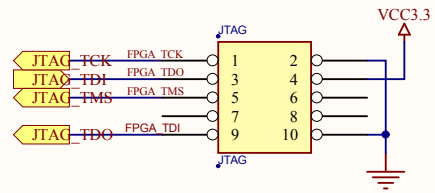
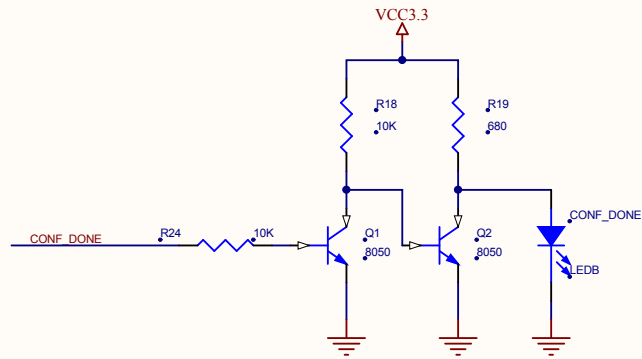
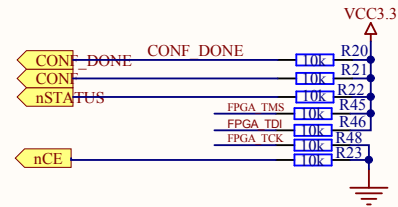
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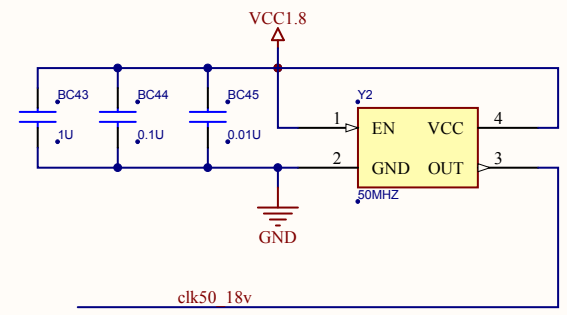
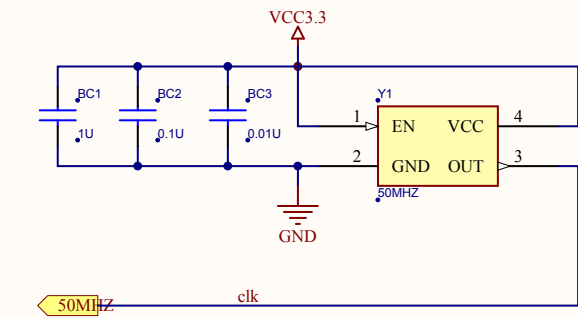
BANK 8

IO, DIFFIO\_T24p, (DQ5T/CQ3T#DPCLK10)(DQ5T/CQ3T#DPCLK10)(DQ5T/CQ3T#DPCLK10), (PADD17) B10 FLASH\_SRAM\_A18  
 IO, DIFFIO\_T24n, (DQ5T)(DQ3T)(DQ5T), (PADD16) B9 FLASH\_SRAM\_A17  
 IO, DIFFIO\_T19n, (DQ5T)(DQ3T)(DQ5T), (PADD18) B7 FLASH\_SRAM\_A19  
 IO, DIFFIO\_T18n, (DQ5T)(DQ3T)(DQ5T), (PADD19) A6 FLASH\_SRAM\_A20  
 IO, DIFFIO\_T20n, (DQ5T)(DQ3T)(DQ5T), (DATA2) A8 FLASH\_SRAM\_DQ9  
 IO, DIFFIO\_T20p, (DQ5T)(DQ3T)(DQ5T), (DATA3) B8 FLASH\_SRAM\_DQ9  
 IO, DIFFIO\_T19p, (DQ5T)(DQ3T)(DQ5T), (DATA4) B7 FLASH\_SRAM\_DQ4  
 IO, (DQ3T)(DQ3T)(DQ5T), (DATA5) A5 FLASH\_SRAM\_DQ6  
 IO, DIFFIO\_T8p, (DQ3T)(DQ3T)(DQ5T), (DATA6) F10 FLASH\_SRAM\_DQ6  
 IO, DIFFIO\_T7n, (DQ3T)(DQ3T)(DQ5T), (DATA7) E6 FLASH\_SRAM\_DQ7  
 IO, DIFFIO\_T6p, (DQ3T)(DQ3T)(DQ5T), (DATA8) F8 FLASH\_SRAM\_DQ9  
 IO, DIFFIO\_T5n, (DQ3T)(DQ3T)(DQ5T), (DATA9) A3 FLASH\_SRAM\_DQ10  
 IO, DIFFIO\_T4n, (DQ3T)(DQ3T)(DQ5T), (DATA10) B3 FLASH\_SRAM\_DQ11  
 IO, DIFFIO\_T4p, (DQ3T)(DQ3T)(DQ5T), (DATA11) C4 FLASH\_SRAM\_DQ12  
 IO, DIFFIO\_T3p, (DQ3T)(DQ3T)(DQ5T), (DATA12) C7 FLASH\_SRAM\_DQ13  
 IO, DIFFIO\_T16p, (DM3T/BWS#5T)(DM3T/BWS#5T)(DM3T/BWS#5T), (DATA13) F8 FLASH\_SRAM\_DQ14  
 IO, DIFFIO\_T16n, (DQ3T/CQ3T#DPCLK11)(DQ3T/CQ3T#DPCLK11)(DQ3T/CQ3T#DPCLK11), (DATA14) C8 FLASH\_SRAM\_DQ14  
 IO, DIFFIO\_T18p, (DQ3T)(DQ3T)(DQ5T), (DATA15) B6 FLASH\_SRAM\_DQ15  
 IO, DIFFIO\_T25n, (DQ5T)(DQ3T)(DQ5T) A10 SRAM\_BE\_n0  
 IO, VREFB8N0, A10 SRAM\_BE\_n1  
 IO, DIFFIO\_T26n, (DQ5T)(DQ3T)(DQ5T) E10 E10 JP2\_78  
 IO, DIFFIO\_T26p, G11 G11 JP3\_17  
 IO, VREFB8N1, E9 E9 JP3\_18  
 IO, DIFFIO\_T14n, E11 H11 JP3\_15  
 IO, DIFFIO\_T14p, H10 H10 JP3\_16  
 IO, VREFB8N2, B5 B5  
 IO, DIFFIO\_T8n, G10 G10 JP3\_20  
 IO, DIFFIO\_T6n, (DQ3T)(DQ3T)(DQ5T) A4 A4 JP3\_33  
 IO, DIFFIO\_T5p, G8 G8 JP3\_21  
 IO, VREFB8N3, D6 D6 JP2\_78  
 IO, E7 E7 JP3\_34  
 IO, DIFFIO\_T3n, (DQ3T)(DQ3T)(DQ5T) C3 C3 JP3\_31  
 IO, DIFFIO\_T1n, (DM3T/BWS#3T)(DM3T1/BWS#3T1)(DM3T1/BWS#3T1) E7 F7 JP2\_77  
 IO, DIFFIO\_T1p, E7 G7 JP3\_38  
 IO, PLL2\_CLKOUTn, E9 F9 JP3\_22  
 IO, PLL2\_CLKOUTp, E6 HSMC\_CLKOUT\_n3  
 IO, PLL3\_CLKOUTn, E5 HSMC\_CLKOUT\_p3  
 IO, PLL3\_CLKOUTp, E9 G9 JP3\_17

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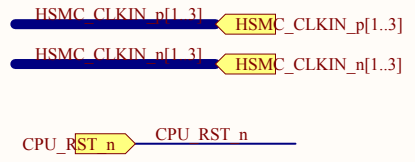




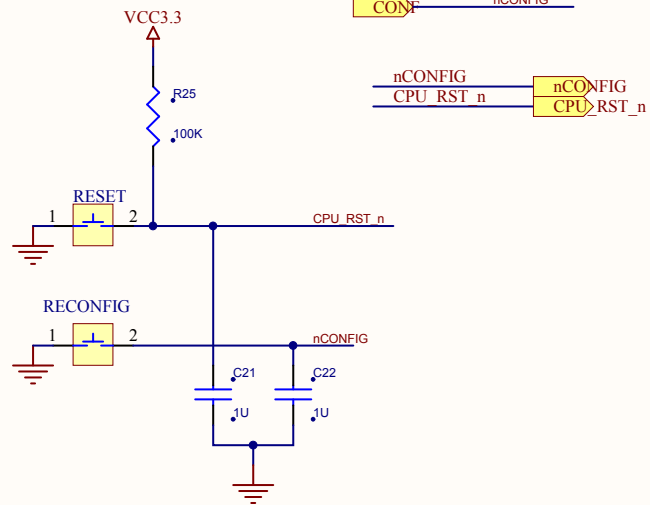
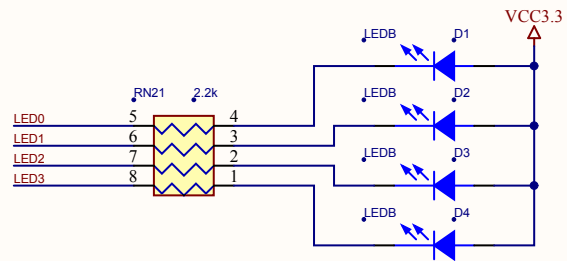
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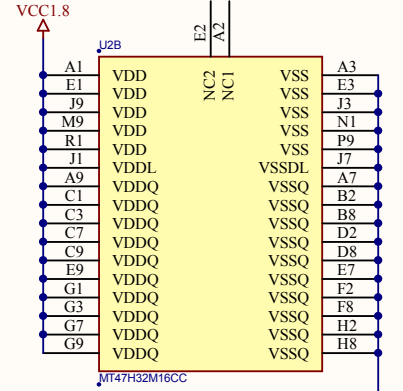
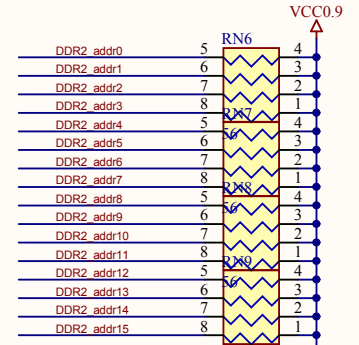
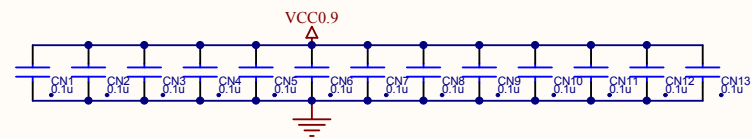
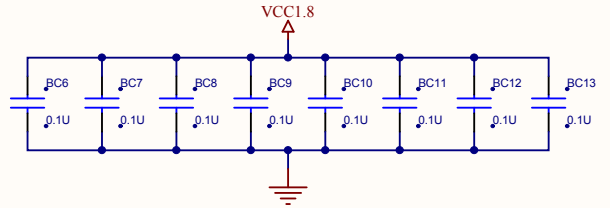
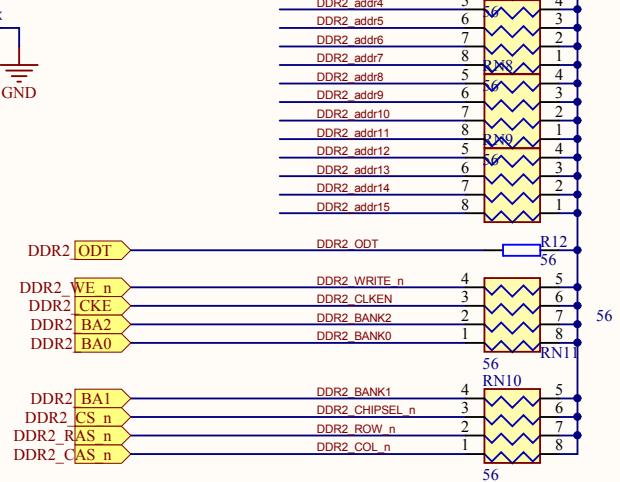
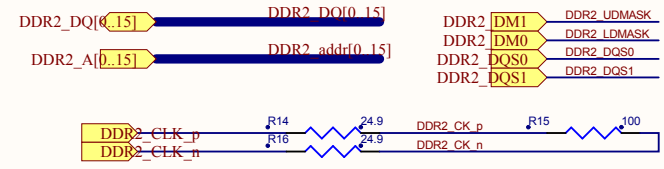
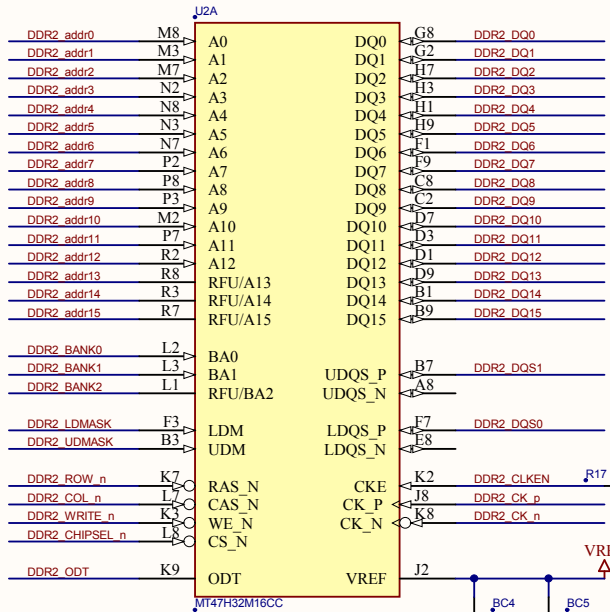
clk0	G2	CLK0, DIFFCLK_0p,(B1)
	G1	CLK1, DIFFCLK_0n,(B1)
	T2	CLK2, DIFFCLK_1p,(B2)
	T1	CLK3, DIFFCLK_1n,(B2)
HSMC_CLKIN_p1	G21	CLK4, DIFFCLK_2p,(B6)
HSMC_CLKIN_n1	G22	CLK5, DIFFCLK_2n,(B6)
HSMC_CLKIN_p2	T21	CLK6, DIFFCLK_3p,(B5)
HSMC_CLKIN_n2	T22	CLK7, DIFFCLK_3n,(B5)
	A12	CLK8, DIFFCLK_5n,(B7)
	B12	CLK9, DIFFCLK_5p,(B7)
HSMC_CLKIN_p3	A11	CLK10, DIFFCLK_4n,(B8)
HSMC_CLKIN_n3	B11	CLK11, DIFFCLK_4p,(B8)
CPU_RST_n	AB12	CLK12, DIFFCLK_7n,(B4)
clk50_18v	AA12	CLK13, DIFFCLK_7p,(B4)
	AB11	CLK14, DIFFCLK_6n,(B3)
clk	AA11	CLK15, DIFFCLK_6p,(B3)

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A

A

B

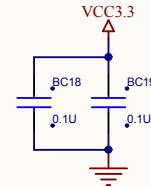
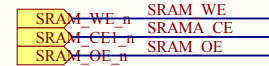
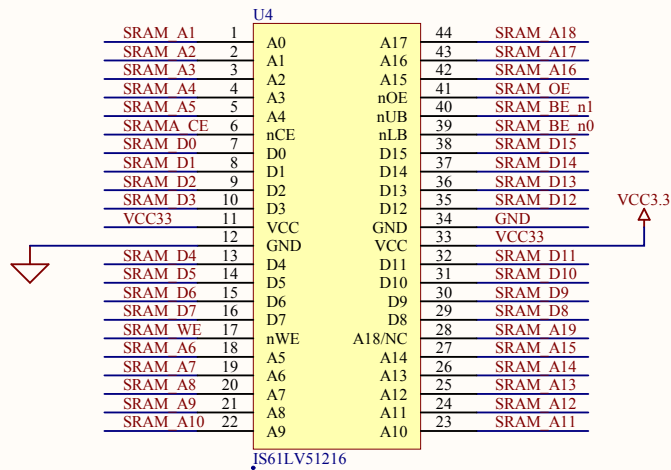
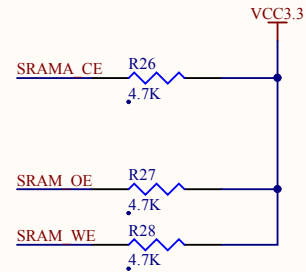
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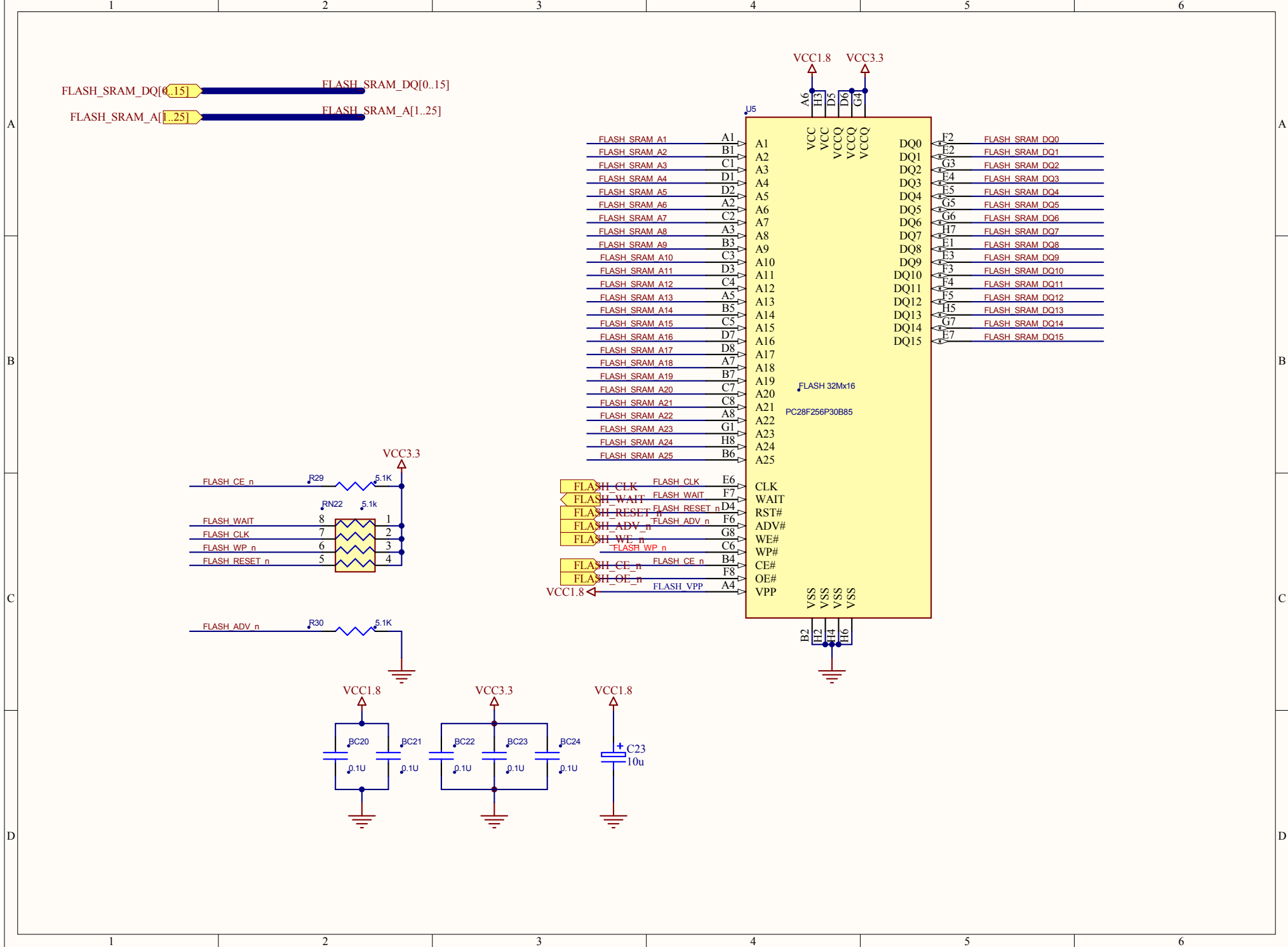
C

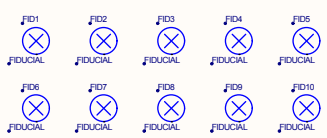
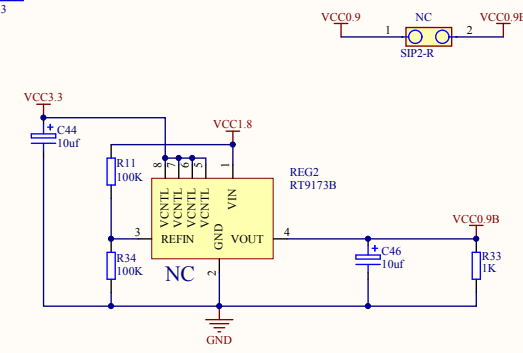
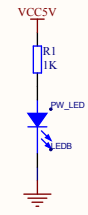
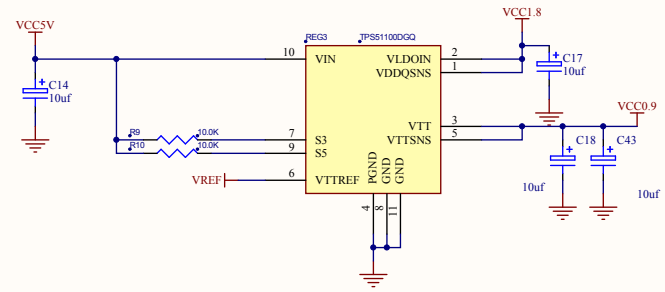
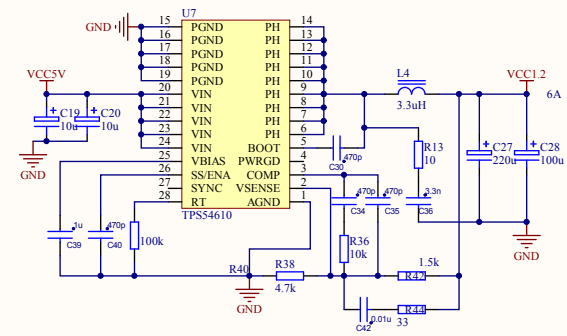
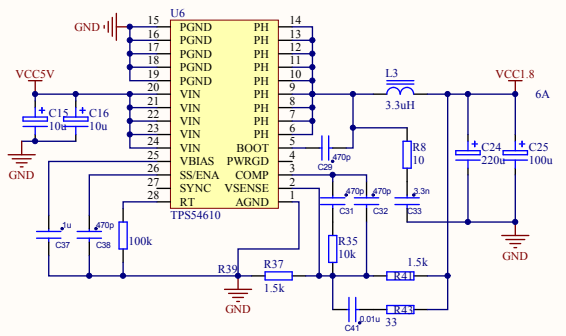
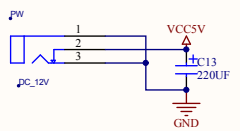
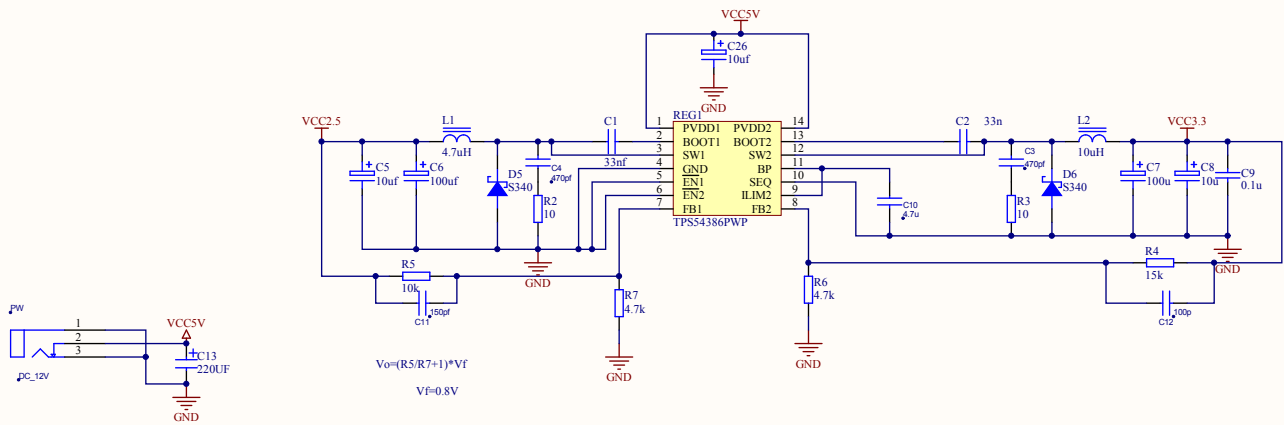
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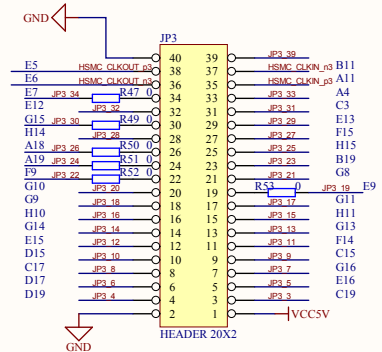
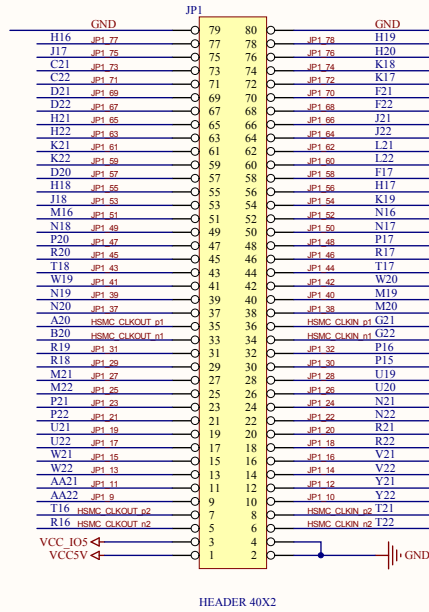
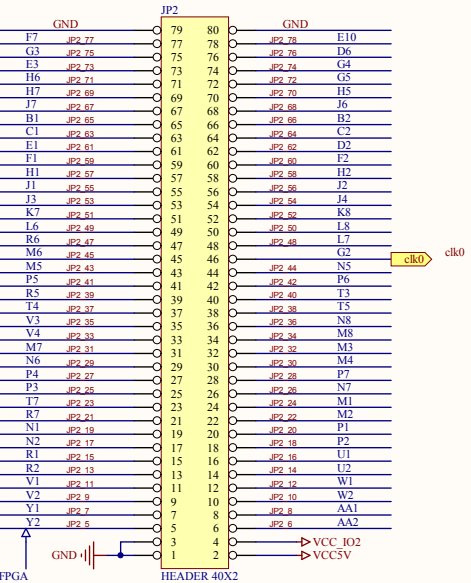
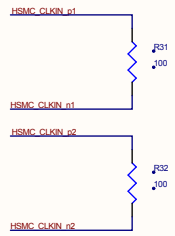
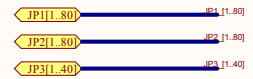
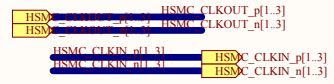
D

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Comment	Description	Designator	Footprint	LibRef	Quantity
1U	1uF, 50V, Y5V, -20~+80%	B1, BC43, C21, C22	C-0603	CAP	4
0.1U	0.1uF, 50V, Y5V, -20~+80%	BC2, BC5, BC6, BC7, BC8, BC9, BC10, BC11, BC12, BC13, BC15, BC17, BC18, BC19, BC20, BC21, BC22, BC23, BC24, BC44, PC1, PC2, PC3, PC4	C-0603	CAP	24
0.01U	10uF, 50V, Y5V, -20~+80%	BC3, BC45	C-0603	CAP	2
0.001U	1mF, 50V, X7R, +/-10%	BC4, BC14, BC16	C-0603	CAP	3
0.1U	0.1uF, 25V, Y5V, -20~+80%, Capacitor	BC25, BC26, BC27, BC28, BC29, BC30, BC31, BC32, BC33, BC34, BC35, BC36, BC37, BC38, BC39, BC40, BC41, BC42, C1, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46	C0603	CAP_CAP_1	43
33nf		C1	C0603	CAP	1
33n		C2	C0603	CAP	1
470pf		C3, C4	C0603	CAP	2
100uf	Electrolytic Capacitor	C5, C14, C17, C18, C26, C43, C44, C46	my3216	ELECTRO1	6
100uf	Electrolytic Capacitor	C6	CT-100	ELECTRO1	1
100u	Electrolytic Capacitor	C7	ct-100	ELECTRO1	1
10u	Electrolytic Capacitor	C8, C15, C16, C19, C20, C23, PC5, PC6, PC7, PC8	my3216	ELECTRO1	10
4.7u		C10	C0603	CAP	1
150pf		C11	C0603	CAP	1
100p		C12	C0603	CAP	1
2200pF		C13	CT-100	CAP1+	1
220u	Electrolytic Capacitor	C24, C27	ct-100	ELECTRO1	2
100u	Electrolytic Capacitor	C25, C28	my3216	ELECTRO1	2
470p		C29, C30, C31, C32, C34, C35, C38, C40	C0603	CAP	6
3.3n		C33, C36	C0603	CAP	2
1u		C37, C39	C0603	CAP	2
0.01u		C41, C42	C0603	CAP	2
LEDB	Blue light SMD, 75mW	CONF, D0NE, D1, D2, D3, D4, PWR, LED	LED0805	LED	6
S340		D5, D6	D	SchottkyDiode	2
FIDUCIAL	NA	FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8, FID9, FID10	FID35R	FIDUCIAL	10
SINGLE_3		J3, J4	SIP5	SINGLE_3	2
HEADER 40X2		JP1, JP2	ICD0-S-SMD	HEADER 40X2	2
HEADER 20X2		JP3	ICD20X2	HEADER 20X2	1
JTAG	BOX Header, MA, ST, BLACK, DIP, 2*3 PIN, 72.54 mm, 8.8 mm	JTAG	CON-2XMM_2	HEADER 2X5	1
4.7uH		L1	L_0603	INDUCTOR	1
10uH		L2	L_0603	INDUCTOR	1
3.3uH		L3, L4	L_0603	INDUCTOR	2
SIP2-R		NC	CN-SMD	SIP2-R	1
DC_12V	DC JACK, 3 PIN, BLACK, 0V, Size: 8.85*14.4*10.7 mm, 2.0 mm	PW	JACK_DC_2MM	Jack-DC	1
B050	UT080505, 20V, 700mA, Pin(1,3,2) = E,B,C	Q1, Q2	SOT-23	BJT-npn	2
1k		R1, R33	my0603	R	2
10		R2, R3, RR, R13	my0603	R	4
10k		R4	my0603	R	1
10k		R5, R20, R21, R22, R23, R35, R36, R45, R46, R48	my0603	R	10
4.7k		R6, R7, R26, R27, R28, R29	my0603	R, RES1	6
10.0K	RES, 10.0K, 0.1%, 1/16W, 0402	R9, R10	my0603	RESISTOR	2
100K		R11, R34, R39, R40	my0603	R	4
50		R12	my0603	R	1
24.9	24.9 ohm, 1/10W, +/-1%	R14, R16	R-0603	RES_Dup1	2
100	100 ohm, 1/10W, +/-5%	R15, R31, R32	R-0603	RES_Dup1	3
10K	10K ohm, 1/10W, +/-5%	R17, R18, R24	R-0603	RES_Dup1	3
680	680 ohm, 1/10W, +/-5%	R19	R-0603	RES_Dup1	1
100K	5.1K ohm, 1/10W, +/-5%	R25	R-0603	RES_Dup1	1
5.1K	5.1K ohm, 1/10W, +/-5%	R29, R30	R-0603	RES_Dup1	2
1.5k		R37, R41, R42	my0603	R	3
33		R43, R44	my0603	R	2
0		R47, R49, R50, R51, R52, R53	my0603	R	6
RECONFIG	RECONFIG	RECONFIG	SMD_SWITCH	SWITCH	1
TPS43860PWP	REG1	REG1	SSOP14	TPS43860PWP	1
RT9173B	REG2	REG2	SOIC-8	RT9173B	1
TPS51100DGG	REGULATOR_3A, SINKSOURCE, DDR, TERMINATION, MSOP, 10 PIN	REG3	PSOP-DGG10	TPS51100	1
RESET	RESET	RESET	SMD_SWITCH	SWITCH	1
50		RN6, RN7, RN8, RN9, RN10, RN11	RP4	RA	6
2.2k		RN21	RA-VEX-0603.8	RA	1
5.1k		RN22		RA	1
EP3K0F484	EP3K16F484	U1	FBGA484-3	EP3K0F484	1
MT47H32M16CC	IC DDR2 SDRAM, 32M x 16 x 8 BANKS, 333MHz CAS LATENCY, 4 FBGA PACKAGE, 84 PINS, 1.8V CORE, 1.8V IO	U2	FBGA84	MT47H32M16CC	1
RClamp0514M		U3	mso10	RClamp0514M	1
IS61LV9216		U4	SOP44, SR256	IS61LV9216	1
FLASH 32Mx16		U5	EASY_BGA_64	FLASH 32Mx16	1
TPS54610		U6, U7	HTSSOP28	TPS54610	2
50MHz	CMOS Oscillator, 50MHz	Y1, Y2	OSC-5X7mm	OSC	2